

In re Patent Application of:
ROCHE
Serial No. 09/479,105
Filing Date: JANUARY 7, 2000

REMARKS

Applicant would like to thank the Examiner for the thorough examination of the present application and for the Examiner interview of June 6, 2005. During the interview, Applicant's attorney highlighted that the claims recite the password as being provided over the data bus, while the Examiner characterized the address provided over the address bus in the Banno et al. patent as the password. The patentability of the claims is discussed in greater detail below. Favorable reconsideration is respectfully requested.

I. The Claimed Invention

Independent Claim 10, for example, recites a microprocessor comprising an address bus, a data bus, a plurality of read and write accessible registers connected to the data bus, and an address decoder connected to the address bus for selecting the plurality of registers as a function of an address provided by the address bus. The microprocessor further comprises a plurality of protection circuits connected between the address decoder and the plurality of registers. Each protection circuit is associated with a register to secure access thereto by blocking selection of the register after each resetting of the microprocessor. The protection circuit is released by a successive sending on the data bus N passwords proper to the register during N first operations for selection of the register, with $N \geq 1$. The selection of the associated register is effective only for subsequent operations for the selection thereof until a next resetting of the microprocessor. Independent Claim 37 is a method counterpart of Claim 10.

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Independent Claim 19 is similar to independent Claim 10 and further recites that a register is blocked during write access operations after each resetting of the microprocessor.

Independent Claim 26 is also similar to independent Claim 10 but further recites, at least two passwords are provided to each register.

II. Claims 10-42 Are Patentable

The Examiner rejected independent Claims 10, 19, 26, and 27 as unpatentable over the Banno et al. patent. The Examiner correctly notes that the Banno et al. patent discloses at column 4, lines 48-55, and in FIGS. 1 and 2, an internal program memory read protection circuit 12 comprising an address decoder 12a connected to the address bus 15, a memory element 12b, and an AND gate 12c.

Independent Claim 10, for example, recites an address bus, a data bus, and a plurality of read and write accessible registers connected to the data bus. In other words, the address bus and data bus are two separate claim elements. Further, the claim recites a protection circuit associated with a register for securing access thereto by blocking selection of the register, and the protection circuit is released by a successive sending on the data bus of N passwords proper to the register. The claimed protection circuit is therefore responsive to a password sent on the data bus. The Banno et al. patent fails to disclose such because the internal program memory read protection circuit 12 of FIG. 2 is responsive to the address bus 15 or to the instruction execution unit 11d, but not the data bus 16. Independent Claims 19, 26, and 37 include similar features to Claim 10.


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Accordingly, independent Claims 10, 19, 26, and 37 are patentable. Their dependent claims, which recite yet further distinguishing features, are also patentable over the prior art and require no further discussion herein.

CONCLUSION

In view of the arguments provided herein, it is submitted that all the claims are patentable. Accordingly, a Notice of Allowance is requested in due course. Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,


DOUGLAS J. VISNIUS
Reg No. 48,012
Allen, Dyer, Doppelt, Milbrath
& Gilchrist, P.A.
255 S. Orange Avenue, Suite 1401
Post Office Box 3791
Orlando, Florida 32802
407-841-2330

CERTIFICATE OF FACSIMILE TRANSMISSION

I HEREBY CERTIFY that the foregoing correspondence has been forwarded via facsimile number 571-273-8300 to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 this 2nd day of August, 2005.

